REMARKS

In response to the Examiner's Action mailed October 19, 2001, Applicants amend their application and request reconsideration. In this Amendment, claim 10 and non-elected claims 14-17 are cancelled, leaving examined claims 1-9 and 11-13 pending.

A more descriptive title is voluntarily submitted in this Amendment.

The invention concerns a field effect transistor structure that is particularly useful in a relatively high power amplifier operating at high frequencies. The transistor generally includes a gallium arsenide or other compound semiconductor substrate and a plurality of source, drain, and gate electrodes arranged sequentially on that substrate in an active region of the substrate. The respective gates, sources, and drains are connected in parallel in order to increase the output power capacity of the field effect transistor structure. The connection of either the source or drain electrodes includes an air bridge to pass over other wiring without contact. In some illustrated embodiments of the invention, the source wiring includes air bridges, and in other illustrated embodiments, air bridges connect drain electrodes. To this extent, the structure disclosed is mostly conventional.

The disclosed structures are unconventional with regard to a number of features. For example, in the basic embodiment illustrated in Figures 1-3 of the patent application, the channel regions include two ninety degree bends as do the gate electrodes and source and drain electrodes. As explained in the patent application, this bending allows reduction in size of the field effect transistor structure. In the embodiment illustrated in Figures 4 and 5, the active region of the substrate includes insulating regions 14a disposed directly opposite the bent portions, i.e., at the bending positions, of the gate electrodes. The illustrated embodiment includes two such bends and, therefore, two stripe-like insulating regions, but a structure including a larger number of bends in each gate electrode would include a larger number of insulating regions.

Far more complex embodiments according to the invention are illustrated in Figures 6-12 of the patent application. In those structures, the gate electrodes and the drain electrodes include multiple bends and pass adjacent rectangular or square regions including the source electrodes and via hole connections to the rear surface of the structure for grounding. The described structures may include additional air bridges and

insulating regions to improve performance at the high frequencies at which these structures typically operate.

In Figures 13-16, yet another embodiment is illustrated. In addition to the structures shown in some of the other figures, a gate pad 24 and a drain pad 28 respectively provide connections to the gate and drain electrodes at their bending positions, i.e., where they change direction by essentially ninety degrees.

Claim 1 is a generic claim and encompasses the embodiment of Figure 1 as well as the other depicted embodiments. Claims 2 and 3 are also supported by the embodiment of Figure 1. Claims 4-6 are supported by the embodiment of Figure 4. Claims 4 and 6 have identical limitations which have been clarified to explain the location of the insulating regions opposite the bending positions of the gate electrodes. The clarified claims are entirely consistent with the embodiment of Figures 4 and 5. The same figures also support claim 7 which has been clarified, consistent with the described embodiments, as well. Claim 8 is supported by all of the embodiments described in the patent application. Claim 8 requires that each gate electrode have at least two bending positions whereas claim 1 only requires one such bending position within each gate electrode. Claim 8 makes clear that the bends are all essentially ninety degrees. Claim 9 is supported by the embodiment of Figures 13 and 14. In that embodiment, the common pad electrode 24 is connected to the bending positions of each of the first and second gate electrodes. The remaining claims 10-13 are supported by all described embodiments.

Although the initial entry in the Official Action at page 2 is somewhat ambiguous, the detailed comments of the Official Action indicate that all of the examined claims 1-13 were rejected as unpatentable over Tsutsui (U. S. Patent 5,925,901) in view of Tozawa (Japanese Published Patent Application Hei. 3-270024). This rejection is respectfully traversed.

Applicants do not quarrel with the Examiner's characterization of Tsutsui, a disclosure quite similar to the description of the prior art included in this patent application. Tsutsui does not describe any gate electrodes nor channel regions that include bends. For disclosure of gate electrode bends of "essentially ninety degrees", the Examiner relied upon Tozawa. That reliance is erroneous.

Applicants readily agree that Tozawa describes a structure that is similar to the Tsutsui field effect transistor structure but one that includes bends in each of the source, gate, and drain electrodes where they are disposed on the active region of the substrate. According to the Examiner's characterization, Tozawa "describes first and second channel regions having width directions substantially perpendicular to each other". The basis for the Examiner's conclusion is not explained. It is apparent from inspecting Figure 1(a) of Tozawa that the bends in the source, gate, and drain electrodes are not anywhere close to ninety degrees. Perhaps the Examiner is interpreting the modifier "substantially" in the examined claims excessively broadly as to include a very wide range of angles. Applicants respectfully disagree with such an interpretation. To avoid that interpretation, the term "substantially" is changed in the claims to "essentially". The term "essentially" means that while the angle may slightly deviate from ninety degrees, it may not greatly deviate from ninety degrees. Clearly, the structure in Tozawa includes bends that are significantly different from ninety degrees.

The angular bend of the gate electrodes and the corresponding bends between channel regions in the invention and Tozawa does determine the degree of space saving in the respective field effect transistor structure. However, the choice of that angle in the invention is not arbitrary, as described in the patent application.

> The reason why the gate electrode (18), etc. are bent 90° in the FET chip (10) is that, generally, the compound semiconductor materials such as gallium arsenide and the like show electrical characteristics isotropic in two directions which intersect orthogonally to each other. Therefore, in the structure having the bending angles at 90°, the electrical characteristics of the FET chip (10) do not change because of the bending direction of the gate electrode (18), etc., so that ununiform operation of the FET chip (10) can be prevented. (Specification from page 28, line 18, through page 29, line 2.)

In other words, the choice of the ninety degree angle in combination with the use of an isotropic compound semiconductor substrate provides critically important advantages in the invention. Since Tozawa's gate electrodes and, therefore, its channel regions do not have a ninety degree bend, even though Tozawa employs an isotropic compound semiconductor substrate, clearly Tozawa cannot suggest the invention. Stated another way, the modification of Tsutsui with Tozawa still would not include all of the

features of the invention and particularly the important angular relationship of the gate electrode bending positions and, therefore, could not suggest any claim now pending. Upon reconsideration, on this ground alone, the rejection of all pending claims should be withdrawn.

Although not necessary to demonstrate patentability, it is apparent that, independent of the patentability of claim 1, many of the dependent claims are patentable over the asserted combination of Tsutsui and Tozawa. For example, claims 4 and 6, which have identical limitations although depend from different claims, have a structure not illustrated nor suggested in either of Tsutsui or Tozawa. According to the Examiner, both Tsutsui and Tozawa describe insulating regions on a semiconductor substrate under the bending portion of the first gate electrode and the bending portion of the second gate electrode. Attention was directed to Figures 7 and 8 and element 4, shown only in Figure 8 not in Figure 7, of Tsutsui. However, Tsutsui is clearly free of any electrodes having bent portions so it is not understood how the Examiner could draw this conclusion. There is insufficient detail in order to understand the reference to Figure 2 of Tozawa and this rejection. Tozawa does not, in any event, disclose insulating stripes in the substrate opposite the bends of the electrodes. Therefore, the rejection is plainly erroneous, particularly in view of the clarifying amendments made to claims 4 and 6. The rejection cannot be properly maintained.

With regard to claim 8, it is apparent that two bends are present within the gate electrodes of Tozawa. However, one of those bends is not within the active part of the field effect transistor structure and could easily be eliminated by simple adjustment of the position of the electrode connections to the corresponding gate, source, and drain pads. In other words, the second bend in Tozawa is superfluous and without function. In any event, neither of the two bends in Tozawa is essentially a ninety degree bend and, therefore, the limitation of claim 8 cannot be met by any combination of Tsutsui and Tozawa.

Claim 9 specifies that the connections to the first gate electrode and the second gate electrode are made to a common pad electrode at the bending positions of the first gate electrode and the second gate electrode. The Examiner stated that such a connection is illustrated in Figures 1(a) and 2 of Tozawa. This position strains credulity. There are

no bends in the electrodes of the field effect transistor structure of Figure 2 of Tozawa unless one considers, contrary to all common understanding in the art, that the pads commonly connecting similar electrodes in Tsutsui comprise bending portions. The only basis for the rejection of claim 9 is a misinterpretation of the claim, an interpretation that is not supported by the prior art nor common usage in the art.

Finally, with respect to claims 12 and 13, lumped together by the Examiner, the characterization of what is shown in Tozawa is totally contrary to the disclosure of Tozawa. Claim 12 specifies that the first gate electrode has a ninety degree bend at the bending position. Nothing has a ninety degree bend in Tozawa and the Examiner is invited to apply a protractor to Figure 1(a) of Tozawa to test that statement. Further, as to claim 13, no angle that is substantially forty-five degrees to the longer side of the active region is formed by any of the electrodes in Tozawa. This conclusion, which led to the rejection of claim 13, is founded on the same error that led to the rejection of claim 12. If the Examiner is relying upon some passage in the text of Tozawa that is different from what is shown in the figures of Tozawa, then he is invited to provide detailed explanation of that reliance. Otherwise, the Official Action has failed to establish *prima facie* obviousness as to not only these claims 12 and 13 but as to all claims pending in this patent application.

Reconsideration and withdrawal of the rejection and allowance of claims 1-9 and 11-13 are earnestly solicited.

Respectfully submitted,

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PATENT
Attorney Docket No. 400762/Aoyama

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SUZUKI et al.

Application No.:	09/613,749	Art Unit:	2814
Filed:	July 11, 2000	Examiner:	S. Rao

For: SEMICONDUCTOR DEVICE

SPECIFICATION, CLAIMS, AND ABSTRACT AS AMENDED IN RESPONSE TO THE OFFICIAL ACTION MAILED OCTOBER 19, 2001

Amendments to existing claims:

1. (Twice Amended) A semiconductor device comprising:

(a) ~~a~~ an electrically isotropic compound semiconductor substrate having a first surface and a second surface;

(b) an active region on the first surface of the substrate;

(c) a first semiconductor element in the active region, including

first and second channel regions having width directions ~~substantially~~ essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first and second channel regions and opposing each other with the first and second channel regions therebetween, and in ohmic contact with the active region, and

a first gate electrode on the first and second channel regions and along the first source electrode and the first drain electrode, and bent at at least one bending position; and

(d) a second semiconductor element on the active region adjacent to the first semiconductor element, including

third and fourth channel regions adjacent to the first and second channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

one of a second source electrode and a second drain electrode opposing the first drain electrode or the first source electrode [through] across the third and fourth channel regions, and in ohmic contact with the active region, and

a second gate electrode on the third and fourth channel regions and along one of the second source electrode and the second drain electrode, and bent at at least one bending position.

2. (Twice Amended) The semiconductor device according to claim 1, wherein the source electrode and the drain electrode are band-like electrodes, and the bending position of the first gate electrode and the bending position of the second gate electrode lie on a straight line substantially parallel ~~with~~ to a longer side of the active region.

4. (Twice Amended) The semiconductor device according to claim 1, ~~further~~ comprising:

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position;

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth being position; and

first and second insulating regions on the semiconductor substrate and under the first and second bending ~~position~~ positions of the first and second gate ~~electrode~~ electrodes, and under the third and fourth bending ~~position~~ positions of the first and second gate ~~electrode~~ electrodes, respectively.

5. (Twice Amended) The semiconductor device according to claim 1, wherein the first source electrode has a rectangular shape, two sides of which are adjacent to the first and second channel regions, respectively, and wherein the first source electrode is connected to a conductive film on the second surface of the semiconductor substrate~~,~~ through a via-hole in the first source electrode.

6. (Twice Amended) The semiconductor device according to claim 5,~~ further~~ comprising:

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position;

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth being position; and

first and second insulating regions on the semiconductor substrate and under the first and second bending~~ position~~ positions of the first and second gate~~ electrode~~ electrodes, and under the third and fourth bending~~ position~~ positions of the first and second gate~~ electrode~~ electrodes, respectively.

7. (Amended) The semiconductor device according to claim 6, wherein~~ the insulating region is formed so that~~ the width of at least one of the first~~ or~~ and second channel~~ region~~ regions is narrower than the width of the source electrode adjacent~~ to~~ the channel region.

9. (Twice Amended) The semiconductor device according to claim 5, wherein the first gate electrode and the second gate electrode are~~ parallel to~~ spaced uniformly from each other and~~ are connected to~~ including a common pad electrode extending across and connected to the first and second gate electrodes at~~ a~~ the bending position of the first gate electrode and~~ a~~ the bending position of the second gate electrode.

12. (Twice Amended) The semiconductor device according to claim 1, wherein the first gate electrode is bent at a right angle at ~~a~~ the bending position.

13. (Twice Amended) The semiconductor device according to claim 1, wherein an angle formed between ~~a~~ the width direction of the first gate electrode and a longer side direction of the active region is ~~substantially~~ essentially 45°.